CLAIMS

What is claimed is:

1. A circuit comprising:

a processor; and

a memory connected to the processor, said memory storing a plurality of instructions, wherein execution of the instructions by the processor causes:

(a) generating a sequence of binary addresses with a length N, wherein N is greater or equal to a desired sequence length 2D, wherein N is a power of 2;

(b) selecting a combination of 2D addresses from the generated sequence;

(c) checking if the addresses in the selected combination satisfy the property of only one bit difference between consecutive addresses; and

(d) repeating (b) and (c) until a combination of 2D addresses that satisfies the one bit difference property is found.

2. The circuit according to claim 1 wherein D is an arbitrary number.

3. The circuit according to claim 1 wherein D is the depth of a data structure.

4. A method for generating a sequence of binary addresses of length 2D, the method comprising:

(a) generating a sequence of binary addresses with a length N, wherein N is greater or equal to the desired sequence length 2D, wherein N is a power of 2;

(b) selecting a combination of 2D addresses from the generated sequence;

(c) checking if the addresses in the selected combination satisfy the property of only one bit difference between consecutive addresses; and

(d) repeating (b) and (c) until a combination of 2D addresses that satisfies the one bit difference property is found.

5. The method according to claim 4 wherein D is an arbitrary number.

6. The method according to claim 4 wherein D is the depth of a data structure.